PXIe-3117a/3115a

PXI Express Embedded Controller

User's Manual

Manual Rev.: 1.0

Revision Date: Aug. 28, 2024

Revision History

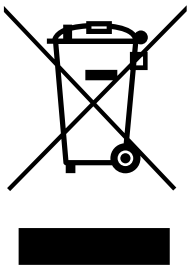
Revision	Release Date	Description of Change(s)
1.0	2024-8-28	Initial release

Preface

Disclaimer

The information in this document is subject to change without prior notice in order to improve reliability, design, and function and does not represent a commitment on the part of the manufacturer.

In no event will the manufacturer be liable for direct, indirect, special, incidental, or consequential damages arising out of the use or inability to use the product or documentation, even if advised of the possibility of such damages.



JYTEK is committed to fulfill its social responsibility to global environmental preservation through compliance with the European Union's Restriction of Hazardous Substances (RoHS) directive and Waste Electrical and Electronic Equipment (WEEE) directive. Environmental protection is a top priority for JYTEK. We have enforced measures to ensure that our products, manufacturing processes, components, and raw materials have as little impact on the environment as possible. When products are at their end of life, our customers are encouraged to dispose of them in accordance with the product disposal and/or recovery programs prescribed by their nation or company.

Battery Labels (for products with battery)

California Proposition 65 Warning

WARNING: This product can expose you to chemicals including acrylamide, arsenic, benzene, cadmium, Tris(1,3-dichloro-2-propyl)phosphate (TDCPP), 1,4-Dioxane, ane, formaldehyde, lead, DEHP, styrene, DINP, BBP, PVC, and vinyl materials, which are known to the State of California to cause cancer, and acrylamide, benzene, cadmium, lead, mercury, phthalates, toluene, DEHP, DIDP, DnHP, DBP, BBP, PVC, and vinyl materials, which are known to the State of California to cause birth defects or other reproductive harm. For more information go to www.P65Warnings.ca.gov.

Trademarks

Product names mentioned herein are used for identification purposes only and may be trademarks and/or registered trademarks of their respective companies.

Conventions

Take note of the following conventions used throughout this manual to make sure that users perform certain tasks and instructions properly.

NOTE: Additional information, aids, and tips that help users perform tasks.

CAUTION: Information to prevent ***minor*** physical injury, component damage, data loss, and/or program corruption when trying to complete a task.

WARNING: Information to prevent ***serious*** physical injury, component damage, data loss, and/or program corruption when trying to complete a specific task.

Table of Contents

This page intentionally left blank.

List of Figures

This page intentionally left blank.

List of Tables

This page intentionally left blank.

1 Introduction

The JYTEK PXIe-3117a/3115a PXI Express embedded controllers are designed to offer a cost-effective solution for hybrid PXI Express-based testing systems while maintaining strong performance. Based on the 9th and 8th generation Intel® Core™ i7/i5 processors, these controllers deliver reliable computing power suited for a variety of testing and measurement applications at a competitive price point.

The PXIe-3117a/3115a are equipped with multi-core processors that allow the efficient execution of multiple tasks simultaneously in a multi-tasking environment. With auto-configured PCIe switches, these controllers support four x4 or two x8 PXI Express links, providing maximum system throughput of up to 16 GB/s through the PCI Express 3.0 bus.

Featuring up to 64 GB of dual-channel DDR4 memory at 2400 MHz (non-ECC), the PXIe-3117a/3115a are engineered to meet the demands of various applications while optimizing costs. The controllers also come with a range of integrated I/O options, including dual USB 3.2 Gen1 ports (5 Gbps), four USB 2.0 ports, dual 1GbE Ethernet ports for LAN connection and LXI instrument control, and an RS232 port. Advanced PXI trigger functionality is enabled through built-in trigger I/O.

The PXIe-3117a, powered by the 9th Gen Intel® Core™ i7-9850HE processor with 6 cores and 12 threads, and the PXIe-3115a, equipped with the 8th Gen Intel® Core™ i5-8400H processor with 4 cores and 8 threads, offer a balance of performance and affordability. These controllers are designed to meet the needs of professionals who require reliable performance in high-stakes testing and measurement scenarios, while optimizing for budget constraints. Whether managing high-speed LAN connections, controlling LXI instruments, or handling peripheral devices, the PXIe-3117a/3115a are ideal for applications where cost-effectiveness and dependable performance are key considerations.

NOTE:

Memory addressing over 4GB is OS-dependent, such that a 32-bit operating system may be unable to address memory space over 4GB. To fully utilize memory, 64-bit operating systems are required.

1.1 Features

- PXI™-5 PXI Express Hardware Specification Rev.1.1
- PXIe-3117a: Intel® Core™ i7-9850HE (Base Frequency 2.7 GHz, Turbo Frequency 4.4 GHz)
  PXIe-3115a: Intel® Core™i5-8400H (Base Frequency 2.5 GHz, Turbo Frequency 4.2 GHz)
- DDR4-2400MHz SODIMM x2
  - Default: 16GB, up to 64GB 2400 MHz
- Maximum System Throughput 16 GB/s
- PXI Express Link Capability
  - Four Link Configuration: x4 x4 x4 x4
  - Two Link Configuration: x8 x8
- NVME M.2 SSD
  - Supports 2280 SSD
  - PCIe Gen3 x 4
- Integrated I/O
  - Dual Gigabit Ethernet ports
  - Two USB 3.2 Ports
  - Four USB 2.0 Ports
  - Dual DisplayPort connectors
  - One COM port (D-sub 9-pin serial)
  - Trigger I/O for advanced PXI™ trigger functions
- OS
  - Microsoft Windows 7/10，Linux 64-bit
  - Linux (Kernel>5.8)

1.2 Specifications

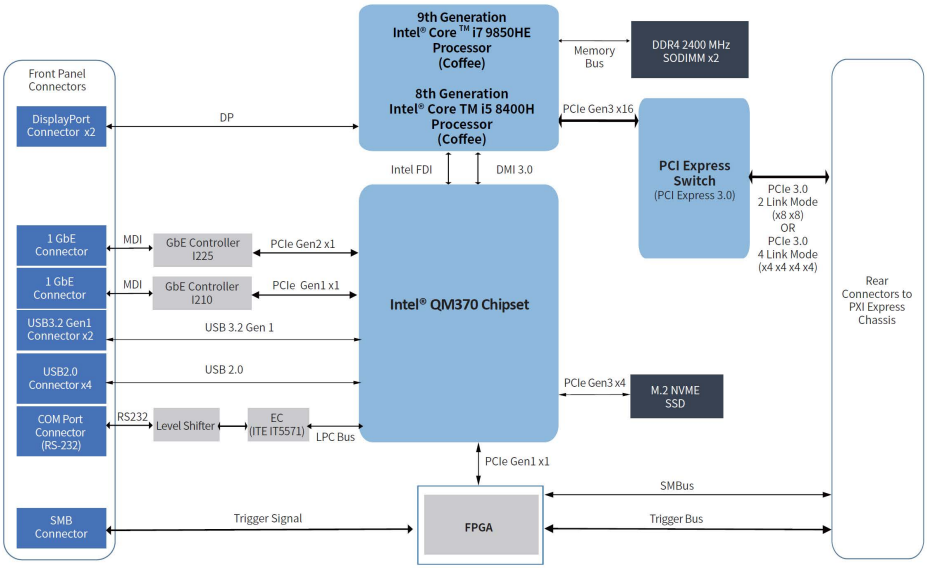


Figure 1-1: Functional Block Diagram

Processor

- Intel® Core™ i7-9850HE/i5-8400H processor

Memory

- Two standard 260-pin DDR4 SODIMM sockets
- Supports 2400 MHz RAM up to 64 GB total
- Supports non-ECC, unbuffered memory

NOTE:

The externally accessible SODIMM socket can accept replacement DDR4 DRAM DIMM modules.
PXIe-3117a/3115a specifications and stability guarantees are only supported when JYTEK-provided DDR4 DRAM SODIMM modules are used.

Video

- DisplayPort supports up to 3840 x 2160 @ 60Hz resolution
- 3840 x 2160 @60Hz DisplayPort adapters to other standards are available,w/max.resolutiondependent on adapter. Support only DisplayPort to HDMI and VGA.


NOTE:

DisplayPort adapters for other standards are available, with maximum available resolution dependent on the adapter chosen

Storage

One NVME M.2 500 GB SSD

I/O Connectivity

Dual Gigabit Ethernet controllers through two RJ45 connectors with speed/link/active LED on the faceplate, with both supporting Wake-on-LAN.

USB

Four USB 2.0 and two USB 3.2 ports on the faceplate.

Trigger I/O

One SMB connector on the faceplate to route an external trigger signal to/from PXI trigger bus

Dimensions (3U PXI module)

3U/4-slot PXI standard

Weight

0.9 kg (exclusive of packaging)

Environmental

Operating temperature with SSD	0 to 55°C
Storage temperature	-40 to 71°C
Relative humidity, non-condensing	5 to 95%

Shock and Vibration

Functional shock 30G, half-sine, 11ms pulse duration

Random vibration:

- Operating 5 to 500Hz, 0.21Grms, 3 axes
- Non-operating 5 to 500Hz, 2.46Grms, 3 axes

Environmental & Shock and Vibration values are only guaranteed with use of an JYTEK provided SSD.

Power Requirements

Typical Consumption	DC +3.3V	DC +5V	DC +12V
Typical operation (Measured while W10 is idle)	4.50 A	0.10 A	1.94 A
Heavy operation (Measured while W10 is under heavy CPU and storage utilization)	6.79 A	4.00 A	7.32 A

1.3 I/O and Indicators

1.3.1 Front Panel

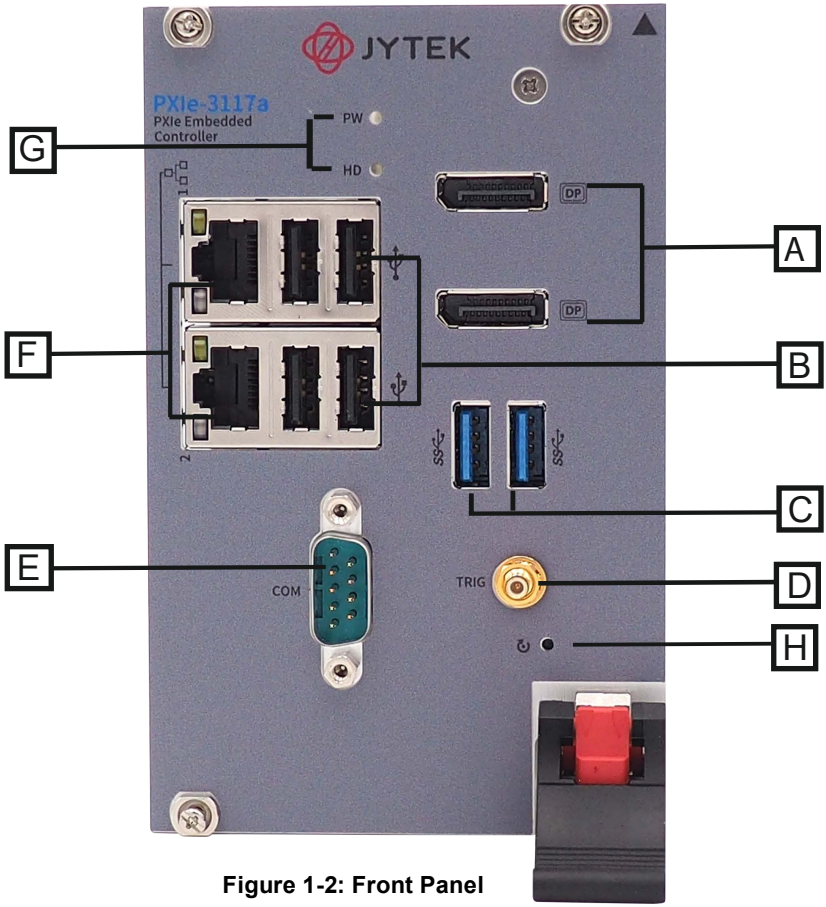


Figure 1-2: Front Panel

A	2x DisplayPort	F	2x Gigabit Ethernet
B	4x Type-A USB 2.0	G	LED indicators
C	2x USB 3.2	H	Reset
D	PXI Trigger		
E	COM port		

Table 1-1: Front Panel Legend

PXI Trigger Connector

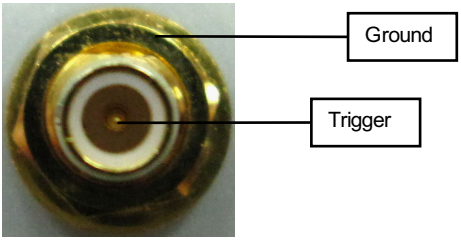


Figure 1-3: PXI Trigger SMB Jack

The PXI trigger connector is an SMB jack, used to route external trigger signals to or from the PXI backplane. Trigger signals are TTL-compatible and edge sensitive. The PXIe-3117a/3115a provides four trigger routing modes from/to the PXI trigger connector to synchronize PXI modules, including

- From a selected trigger bus line to PXI trigger connector
- From the PXI trigger connector to a selected trigger bus line
- From software trigger to a selected trigger bus line
- From software trigger to PXI trigger connector

All trigger modes are programmable by the provided driver.

DisplayPort Connectors

Provides monitor connection for VGA/HDMI monitors; installation of requisite adapters required. Dual display function is also supported.

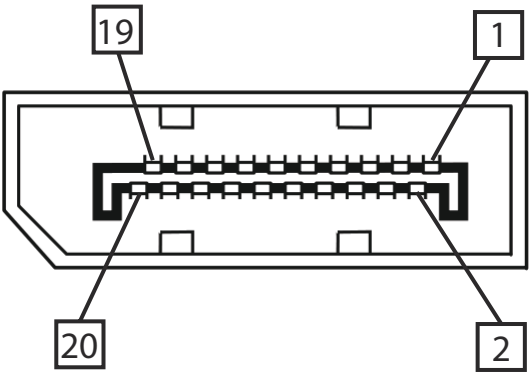


Figure 1-4: DisplayPort Connector

Pin	Signal	Pin	Signal
1	CN_DDPx0+	11	GND
2	GND	12	CN_DDPx3-
3	CN_DDPx0-	13	CN_DDPx_AUX_SEL
4	CN_DDPx1+	14	CN_DDPx_CONFIG2
5	GND	15	CN_DDPx_AUX+
6	CN_DDPx1-	16	GND
7	CN_DDPx2+	17	CN_DDPx_AUX-
8	GND	18	CN_DDPx_HPD
9	CN_DDPx2-	19	GND
10	CN_DDPx3+	20	+V3.3_DDPx_PWR

Table 1-2: DisplayPort Pin Assignment

1.3.2 Reset Button

The reset button, activated by insertion of any pin-like implement, executes a hard reset for the PXIe-3117a/3115a.

1.3.3 LED Indicators

Two LED indicators on the faceplate indicate operational status of the PXIe-3117a/3115a, as follows.

Figure 1-5: LED Indicators

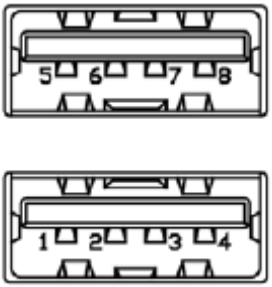
LED	Color	Description
PW	Green	Indicates system power, remaining lit when the system boots normally and main power supply is functioning.
HD	Green	Indicates operating state of the HDD or SSD, flashing during access to or activity on the NVME SSD.

Table 1-3: LED Indicator Legend

1.3.4 USB 2.0 Ports

The PXIe-3117a/3115a provides four USB 2.0 ports via USB Type-A connectors on the faceplate, all compatible with hi-speed, full-speed and low-speed USB devices. Supported boot devices include USB flash drive, USB floppy, USB CD-ROM, and others, with boot priority and device settings configurable in the

BIOS.



Pin	Signal
1/5	Power 5V
2/6	USB Data-
3/7	USB Data +
4/8	Ground

Table 1-4: USB 2.0 Port Pin Assignment

1.3.5 Gigabit Ethernet Ports

Dual Gigabit Ethernet connection is provided on the PXIe-3117a/3115a front panel.

Pin	1000Base-T Signal	100/10Base-T Signal
1	MDI0+	TX+
2	MDI0-	TX-
3	MDI1+	RX+
4	MDI2+	Reserved
5	MDI2-	Reserved
6	MDI1-	RX-
7	MDI3+	Reserved
8	MDI3-	Reserved

Table 1-5: Ethernet Port Pin Assignments

The Ethernet ports each include two LED indicators, one Active/ Link indicator and one Speed indicator, functioning as follows.

LAN1 (1 G)	LED	Status	Description
	Active/Link (Yellow)	Off	Ethernet port is disconnected
		On	Ethernet port is connected with no data transmission
		Flashing	Ethernet port is connected with data transmitted/received
	Speed (Green/ Orange)	Green	100 Mbps
		Orange	1000 Mbps

LAN2 (1G)	LED	Status	Description
	Active/Link (Yellow)	Off	Ethernet port is disconnected
		On	Ethernet port is connected with no data transmission
		Flashing	Ethernet port is connected with data transmitted/received
	Speed (Green/ Orange)	Off	10 Mbps
		Green	100 Mbps
		Orange	1000 Mbps

1.3.6 USB 3.2 Ports

The PXIe-3117a/3115a provides two Type-A USB 3.2 ports on the front panel, supporting SuperSpeed, Hi-Speed, full-speed, and low-speed transmission for downstream. Multiple boot devices, including USB flash, USB external HD, and USB CD-ROM drives are supported, with boot priority configured in BIOS.

NOTE:

USB 3.2 may not be supported by the OS installation programs/ environment. Use USB 2.0 ports for OS installation if necessary.

1.3.7 COM Port

A COM port on the front panel with a D-sub 9-pin connector supports RS-232

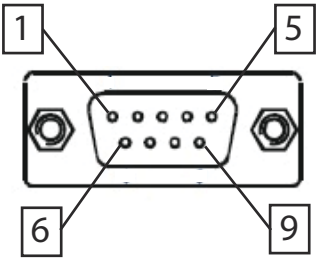


Figure 1-6: COM Port

Pin	Signal Name
	RS-232
1	NC
2	RXD
3	TXD
4	NC
5	GND
6	NC
7	NC
8	NC
9	NC

Table 1-6: D-sub COM Port Signal Functions

1.3.8 Onboard Connections and Settings

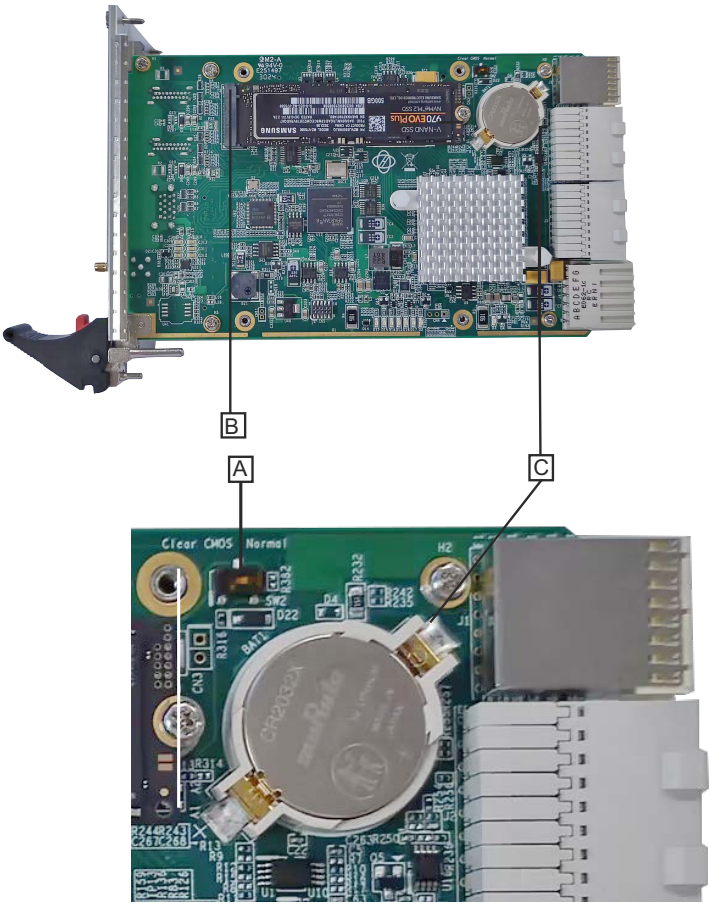


Figure 1-7: Onboard Configuration

A	Clear CMOS switch
B	M.2 connector
C	System battery

Table 1-7: Onboard Configuration Legend

This page intentionally left blank.

2 Getting Started

This chapter describes procedures for installing the PXIe-3117a/3115a and making preparations for its operation, includ-ing hardware and software setup. Please note that the PXIe-3117a/3115a is shipped with RAM and SSD preinstalled. Please contact JYTEK or authorized dealer if there are any problems during the installation.

Diagrams and illustrated equipment are for reference only. Actual system configuration and specifications may vary.

2.1 Package Contents

Before beginning, check the package contents for any damage and ensure that the following items are included:

- PXIe-3117a/3115a Controller (equipped with RAM and. HDD or SSD)
- DP to VGA adapter

If any of these items are missing or damaged, contact the dealer from whom you purchased the product. Save the shipping materials and carton in case you want to ship or store the product in the future.

Do not install or apply power to equipment that is damaged or missing components. Retain the shipping carton and packing materials for inspection. Please contact your JYTEK dealer/ vendor immediately for assistance and obtain authorization before returning any product.

2.2 Operating System Installation

For more detailed information about the operating system, refer to the documentation provided by the operating system manufacturer. Preferred/supported operating systems for PXIe-3117a/3115a are:

- Windows 7, Windows 10， Linux 64-bit
- For other OS support, please contact JYTEK

Most operating systems require initial installation from a hard drive, floppy drive, or CD-ROM drive. The PXIe-3117a/3115a controller supports USB CD-ROM drive, USB flash disk, USB external hard drive, or a USB floppy drive as the first boot device. These devices should be configured, installed, and tested with the supplied drivers before attempting to load the new operating system.

Read the release notes and installation documentation provided by the operating system vendor. Be sure to read all the README files or documents provided on the distribution disks, as these typically note documentation discrepancies or compatibility problems.

1. Select the appropriate boot device order from the BIOS Boot Setup Menu based on the OS installation media used. For example, if the OS is distributed on a bootable installation CD, select USB CD-ROM as the first boot device and reboot the system with the installation CD in the USB CD-ROM drive
2. Proceed with the OS installation as directed and be sure to select appropriate device types if prompted. Refer to the appropriate hardware manuals for specific device types and compatibility modes of JYTEK PXI products.
3. When installation is complete, reboot the system and set the boot device order in the SETUP boot menu accordingly.

2.2.1 Installation Environment

When preparing to install any equipment described in this manual, please refer to Important Safety Instructions.

Only install equipment in well lit areas on flat, sturdy surfaces with access to basic tools such as flat- and cross-head screw-drivers, preferably with magnetic heads as screws and stand-offs are small and easily misplaced.

Recommended Installation Tools include:

- Phillips (cross-head) screwdriver
- Flat-head screwdriver
- Anti-static wrist strap
- Anti-static mat

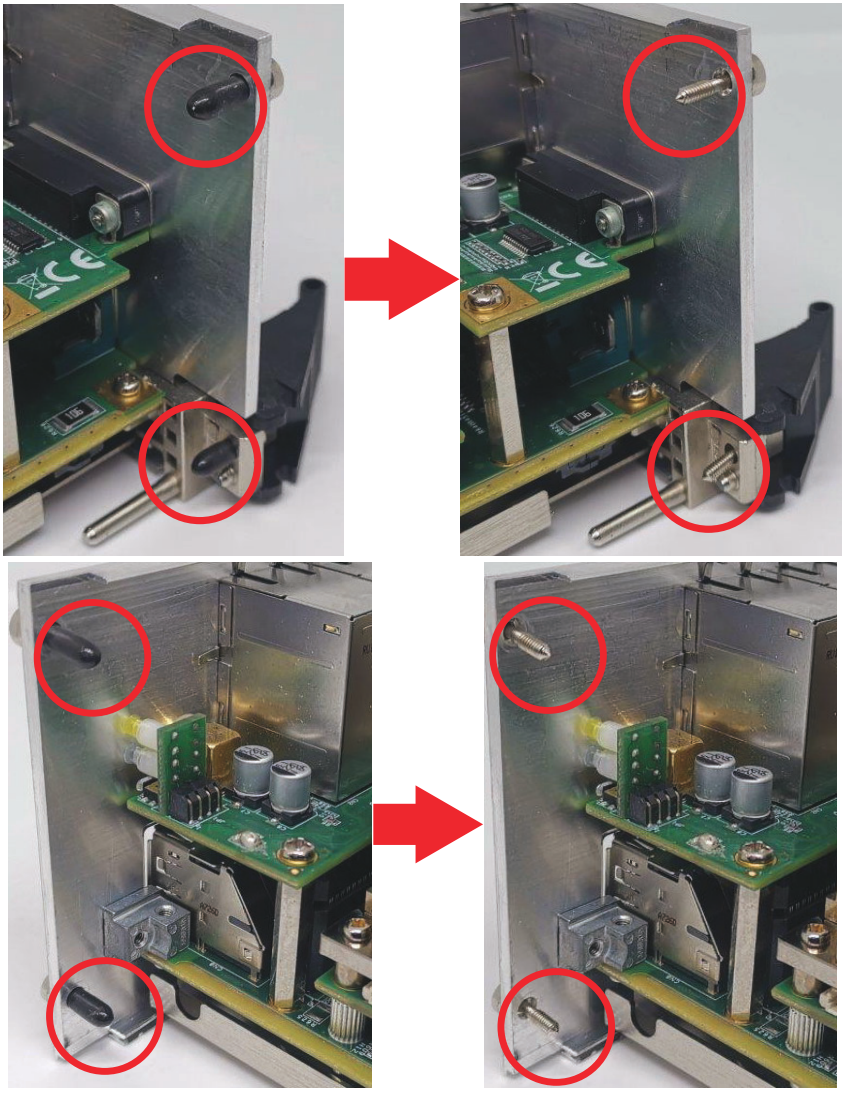
JYTEK PXIe-3117a/3115a system controllers are electrostatically sensitive and can be easily damaged by static electricity. The equipment must be handled on a grounded anti-static mat, and operators must wear an anti-static wristband, grounded at the same point as the anti-static mat.

Inspect the carton and packaging for damage. Shipping and handling may cause damage to the contents. Ensure that all contents are undamaged before installing.

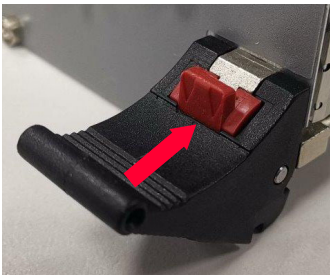
All equipment must be protected from static discharge and physical shock. Never remove any of the socketed parts except at a static-free workstation. Use the anti-static bag shipped with the product to handle the equipment and wear a grounded wrist strap when servicing or installing.

2.2.2 **Installing the** PXIe-3117a/3115a

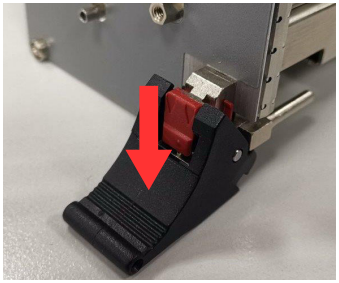
1. Remove all screw caps (x4).



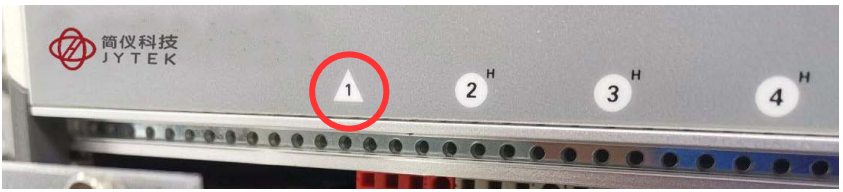
2. Release the red locking lever.



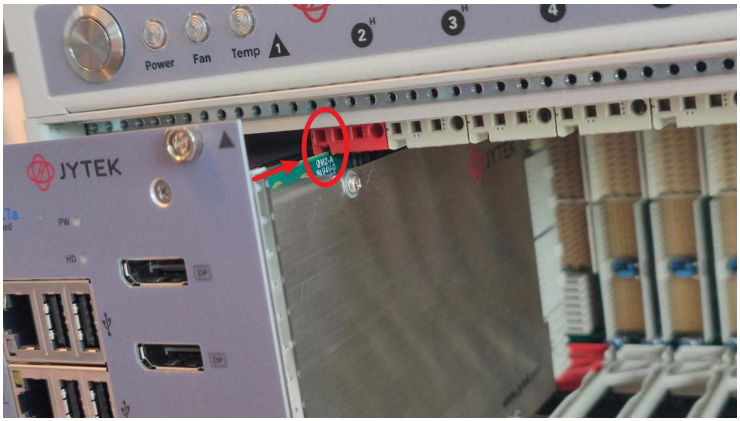
3. Depress the latch.

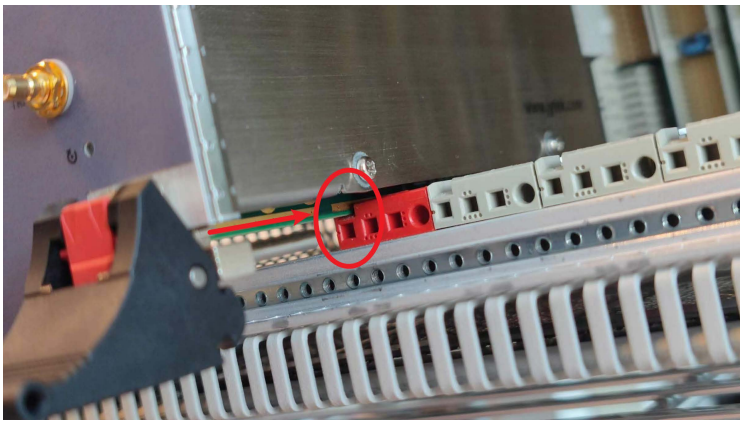


4. Locate the system controller slot on the chassis (Slot 1).



5. Align the controller's top and bottom edges with the card guides and carefully slide the PXIe-3117a/3115a into the chassis, as shown



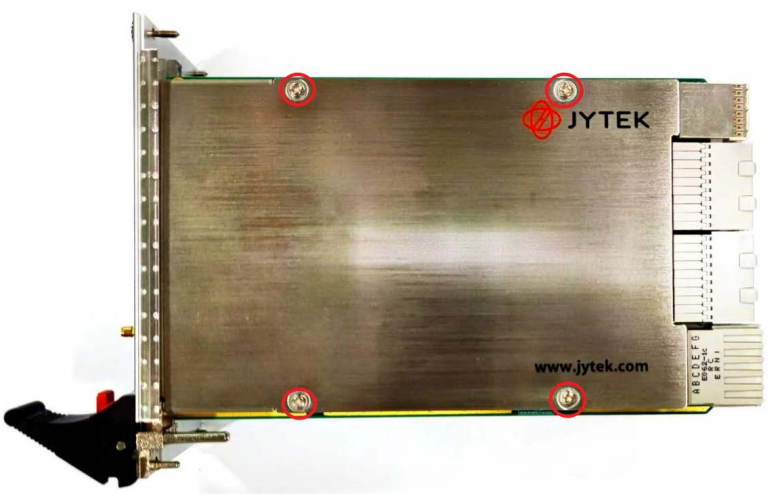


6. Elevate the latch until the PXIe-3117a/3115a is fully seated in the chassis backplane. The alignment pin on the rear of the latch can be threaded into the best fit alignment port in the chassis rail.
7. Fasten the four mounting screws on the faceplate and connect all peripheral devices.

2.2.3 Replacing the Hard Drive or Solid State Drive

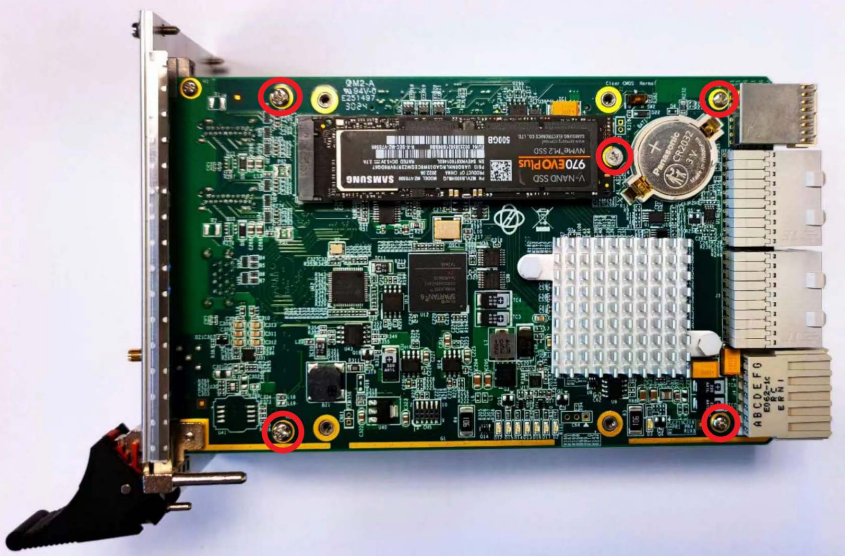
The PXIe-3117a/3115a provides a NVME M.2 port for optional SSD. Installing an SSD is accomplished as follows.

1. Locate the four screws housing to the PXIe-3117a/3115a controller, as shown.



2. Remove the screws.
3. Gently lift and remove the housing.

4. Locate the four screws (two on each side, as shown) fixing the hard drive, and remove.



5. To install an SSD, reverse the steps and reinstall the PXIe-3117a/3115a into the PXI system.

2.2.4 Replacing the Battery Backup

The PXIe-3117a/3115a is provided with a 3.0 V “coin cell” lithium battery, replacement of which is as follows.

1. Turn off the PXI chassis.
2. Remove the PXIe-3117a/3115a embedded controller from the chassis. Observe all anti-static precautions.
3. To remove the battery, gently insert a small (approx. 5 mm) flathead screwdriver under the battery at the negative retaining clip. Gently pry up and the battery should easily pop out.
4. Place a fresh identical battery (CR2032 or equivalent) in the socket, ensuring that the positive pole (+) is facing upwards. The battery is most easily seated by first being inserted under the positive retaining clip, and then pushed downward at the negative retaining clip. The battery should easily snap into position.
5. Reinstall the embedded controller into the PXI chassis and restore power.

2.2.5 Clearing CMOS

In the event of a system malfunction causing the PXIe-3117a/3115a to halt or fail to boot, clear the CMOS and restore the controller BIOS to its default settings. To clear the CMOS:

1. Shut down the controller operating system and turn off the PXI Chassis.
2. Remove the PXIe-3117a/3115a from the chassis. Observe all anti-static precautions.
3. Locate the CMOS clear switch (SW2) on the board (see Section 1.3.8: Onboard Connections and Settings). Move the switch from Normal position

to Clear position

and wait for 5 seconds, then return the switch to Normal position.

4. Remount the controller into the PXI chassis.
5. Press "Delete" to enter the BIOS setup when the splash logo appears.
6. Press "F3" to load Optimized defaults in BIOS setup.
7. Modify the system date and time.
8. Press "F4" to save configuration and exit.

3 Driver Installation

Windows 10 carries most device drivers for the PXIe-3117a/3115a, built-in. Others can be downloaded from the JYTEK PXIe-3117a/3115a Product Page.

After downloading, execute the Setup file, and follow the instructions to complete installation for the following drivers.

- Intel® chipset driver
- Intel® graphics driver
- Intel® Ethernet driver
- Intel® RST driver
- Intel® ME driver
- PXI trigger I/O driver
- JYDM (JYTEK Device Manager, please download JYDM from JYPEDIA)

This page intentionally left blank.

Appendix A - PXI Trigger I/O Function Reference

This appendix describes the use of the PXI trigger I/O function library for the PXIe-3117a/3115a controller, to program routing of trigger signals between the trigger I/O connectors on the faceplate and the PXI trigger bus on the backplane. The API files are located in the installation directory of the PXI Trigger I/O driver.

A.1 Data Types

The PXIe-3117a/3115a library uses the following data types in JYSM_TrigCore.h. It is recommended to use these data types in your application programs. The table below shows the data type names, ranges, and corresponding data types in C/C++, Visual Basic, and Delphi for reference.

Type	Description	Range	C/C++	Visual Basic	Pascal (Delphi)
BOOL	Boolean value	TRUE or FALSE	int	Integer	Boolean
INT8	8-bit signed integer	-128 to 127	signed char	SByte	ShortInt
UINT8	8-bit unsigned integer	0 to 255	unsigned char	Byte	Byte
INT16	16-bit signed integer	-32,768 to 32,767	signed short	Integer	SmallInt
UINT16	16-bit unsigned integer	0 to 65,535	unsigned short	Not supported	Word
INT32	32-bit signed integer	-2,147,483,648 to 2,147,483,647	signed int	Long	LongInt
UINT32	32-bit unsigned integer	0 to 4,294,967,295	unsigned int	Not supported	Cardinal
INT64	64-bit signed integer	-9,223,372,036,854,775,808 to 9,223,372,036,854,775,807	long long	Long	Int64
UINT64	64-bit unsigned integer	0 to 18,446,744,073,709,551,615	unsigned long long	Not supported	UInt64

A.2 Function Library

This section provides detailed definitions of the functions available in the PXIe-3117a/3115a function library. Each function includes a description, list of supported cards, syntax, parameter list, and return code information.

A.2.1 JYSM_Trig_Open

Description

Initializes the trigger I/O function of the PXIe-3117a/3115a controller. This function must be called before the invocation of any other trigger I/O function.

Syntax

C

int JYSM_Trig_Open(const char* systemModuleInstanceName,

JYSM_TrigDeviceHandle* hDevice);

Parameter

systemModuleInstanceName: Name of the system module

instance.

*hDevice: Device handle.

Return Code

0: Success
ErrorCode_SystemModuelNotExist: System module does not exist.
ErrorCode_OpenSystemModuleFailed: Failed to open the system module.

A.2.2 JYSM_Trig_Close

Description

Closes the trigger I/O function of the PXIe-3117a/3115a controller, releasing resources allocated for the trigger I/O function. Users must invoke `JYSM_Trig_Close` before exiting the application.

Syntax

C

int JYSM_Trig_Close(JYSM_TrigDeviceHandle hDevice);

Parameter

hDevice: Device handle.

Return Code

0: Success
ErrorCode_InvalidHandle`: Invalid handle.

A.2.3 JYSM_Trig_SetConfig

Description

Configures the system module trigger lines.

Syntax

C

int JYSM_Trig_SetConfig(JYSM_TrigDeviceHandle hDevice,

JYSM_Trig_Lines line, JYSM_Trig_LineOperatingType opType)

Parameters

hDevice: System module handle.

line: Line to configure.

opType: Line operating type.

Return Code

0: Success
ErrorCode_InvalidHandle: Invalid handle.

A.2.4 JYSM_Trig_GetConfig

Description

Retrieves the configuration of trigger lines.

Syntax

C

```
int JYSM_Trig_GetConfig(JYSM_TrigDeviceHandle hDevice,
JYSM_Trig_Lines line, JYSM_Trig_LineOperatingType* opType);
```

Parameters

hDevice: System module handle.
line: Line to query.
opType: Pointer to the line operating type.

Return Code

0: Success
ErrorCode_InvalidHandle: Invalid handle.

A.2.5 JYSM_Trig_SetValue

Description

Sets a value to a trigger line.

Syntax

C

int JYSM_Trig_SetValue(JYSM_TrigDeviceHandle hDevice, JYSM_Trig_Lines line, BOOL value);

Parameters

hDevice: System module handle.
line: Line to set the value.
value: Value to set (TRUE or FALSE).

Return Code

0: Success
ErrorCode_InvalidHandle`: Invalid handle.

A.2.6 JYSM_Trig_GetValue

Description

Retrieves the value of a trigger line.

Syntax

C

int JYSM_Trig_GetValue(JYSM_TrigDeviceHandle

hDevice, JYSM_Trig_Lines line, BOOL* pValue);

Parameters

hDevice`: System module handle.

line`: Line to query.

pValue: Pointer to store the retrieved value.

Return Code

0: Success
ErrorCode_InvalidHandle: Invalid handle.

A.2.7 JYSM_Trig_SetRouteSignal

Description

Description: Routes trigger signals between trigger lines.

Syntax

C

int JYSM_Trig_SetRouteSignal(JYSM_TrigDeviceHandle hDevice, JYSM_Trig_Lines destLine, JYSM_Trig_Lines sourceLine);

Parameters

hDevice: System module handle.
destLine: Destination line for routing.
sourceLine: Source line for routing.

Return Code

0: Success
ErrorCode_InvalidHandle: Invalid handle.

A.2.8 JYSM_Trig_GetRouteSignal

Description

Retrieves the routing configuration of trigger lines.

Syntax

C

```
int JYSM_Trig_GetRouteSignal(JYSM_TrigDeviceHandle hDevice,
JYSM_Trig_Lines destLine, JYSM_Trig_Lines* sourceLine);
```

Parameters

hDevice: System module handle.
destLine: Destination line to query.
sourceLine: Pointer to store the source line.

Return Code

0: Success
ErrorCode_InvalidHandle: Invalid handle.

Notes

All functions return 0 on success, with various error codes defined for specific failure cases.
The trigger lines (JYSM_Trig_Lines) and operating types (JYSM_Trig_LineOperatingType) are enumerated types that provide predefined values for hardware and software operations.

This page intentionally left blank.

Appendix B Legacy Boot Mode Settings

UEFI boot mode is default for the PXIe-3117a/3115a BIOS.

To boot in legacy boot mode, change related settings in BIOS menu:

1. Power on and press DEL to enter BIOS menu
2. Move to Boot
3. Select CSM Configuration
4. Under “Boot option filter” select “legacy only”
5. Under “Network” select “Legacy”
6. Under “Storage” select “Legacy”
7. Under “Video” select “Legacy”
8. Under “Other PCI devices” select “Legacy”
9. Press F4 and Enter to save and exit BIOS menu. The system will restart and apply settings for Legacy boot mode.

To restore UEFI boot mode:

1. Power on and press DEL to enter BIOS menu
2. Press F3 and Enter to load optimized defaults
3. Press F4 and Enter to save and exit BIOS menu

The system restarts and default settings for UEFI boot mode are applied.

This page intentionally left blank.

Important Safety Instructions

For user safety, please read and follow all instructions, Warnings, Cautions, and Notes marked in this manual and on the associated device before handling/operating the device, to avoid injury or damage.

S'il vous plaît prêter attention stricte à tous les avertissements et mises en garde figurant sur l'appareil , pour éviter des blessures ou des dommages.

- Read these safety instructions carefully
- Keep the User's Manual for future reference
- Read the Specifications section of this manual for detailed information on the recommended operating environment
- The device can be operated at an ambient temperature of 50ºC
- When installing/mounting or uninstalling/removing device; or when removal of a chassis cover is required for user servicing (See "Getting Started" on page 17.):
  - Turn off power and unplug any power cords/cables
  - Reinstall all chassis covers before restoring power
- To avoid electrical shock and/or damage to device:
  - Keep device away from water or liquid sources
  - Keep device away from high heat or humidity
  - Keep device properly ventilated (do not block or cover ventilation openings)
  - Always use recommended voltage and power source settings
  - Always install and operate device near an easily accessible electrical outlet
  - Secure the power cord (do not place any object on/over the power cord)
  - Only install/attach and operate device on stable surfaces and/or recommended mountings
- If the device will not be used for long periods of time, turn off and unplug from its power source

- Never attempt to repair the device, which should only be serviced by qualified technical personnel using suitable tools
- A Lithium-type battery may be provided for uninterrupted backup or emergency power.

Risk of explosion if battery is replaced with one of an incorrect type; please dispose of used batteries appropriately.
Risque d'explosion si la pile est remplacée par une autre de type incorrect. Veuillez jeter les piles usagées de façon appropriée.

- The device must be serviced by authorized technicians when:
  - The power cord or plug is damaged
  - Liquid has entered the device interior
  - The device has been exposed to high humidity and/or moisture
  - The device is not functioning or does not function according to the User's Manual
  - The device has been dropped and/or damaged and/or shows obvious signs of breakage
- Disconnect the power supply cord before loosening the thumbscrews and always fasten the thumbscrews with a screwdriver before starting the system up
- It is recommended that the device be installed only in a server room or computer room where access is:
  - Restricted to qualified service personnel or users familiar with restrictions applied to the location, reasons therefor, and any precautions required
  - Only afforded by the use of a tool or lock and key, or other means of security, and controlled by the authority responsible for the location

	**BURN HAZARD** Touching this surface could result in bodily injury. To reduce risk, allow the surface to cool before touching. ***RISQUE DE BRÛLURES*** *Ne touchez pas cette surface, cela pourrait entraîner des blessures.* *Pour éviter tout danger, laissez la surface refroidir avant de la toucher.*

This page intentionally left blank.

Getting Service

Contact us should you require any service or assistance.

Shanghai Jianyi Technology Co., Ltd.
Web Site http://www.jytek.com
Address: 上海市浦东新区张江高科技园区芳春路300号
300 Fang Chun Rd., Zhangjiang Hi-Tech Park, Pudong New Area, Shanghai,201203,China
Tel: +86-21-5047-5899
Email: service@jytek.com